

Business Issues Having Environmental Health and Safety Ramifications in the Semiconductor Industry.

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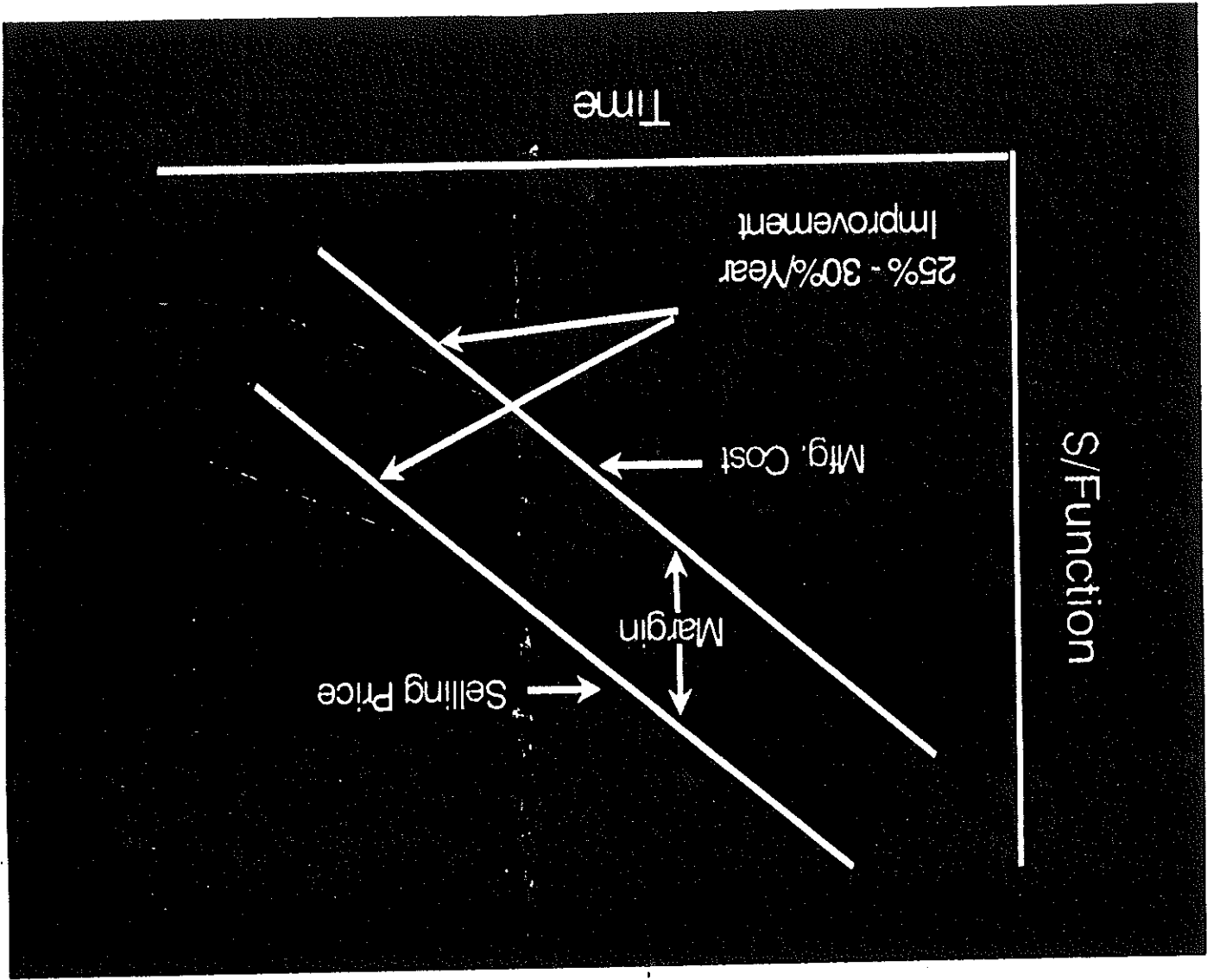
Outline

- I. Semiconductor economics.
 - A. Major factors in semiconductor fab profitability.
 - B. Semiconductor business cycles.
 - C. Semiconductor water fab phases.
 - D. Process life cycles.
- II. Business issues having ESH ramifications at each phase.
 - A. Semiconductor business cycles.
 - B. Semiconductor water fab phases.
 - C. Process life cycles.
 - D. Other.
- III. Current hot issues.
 - A. Global warming.
 - B. Water usage and waste minimization.
 - C. Barriers to international competition.
 - D. Worker safety.

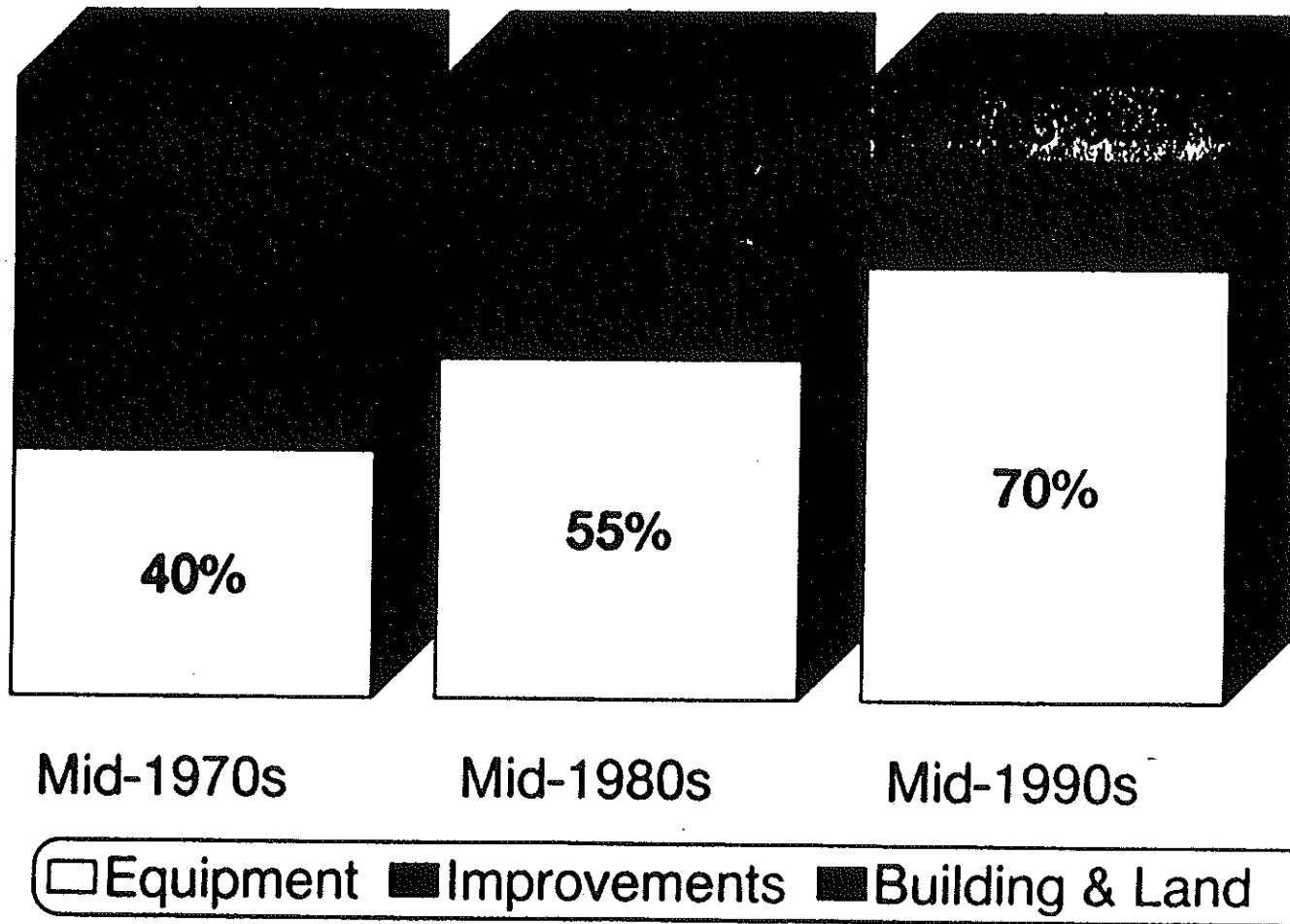
Major Factors In Semiconductor Fab Profitability.

- **Heavy capital expenditures.**
- **Average Selling Price (ASP).**
- **Die yield.**
- **Line yield.**
- **Tool utilization.**

Semiconductor Industry Productivity Expectations.



Process Equipment Dominance.



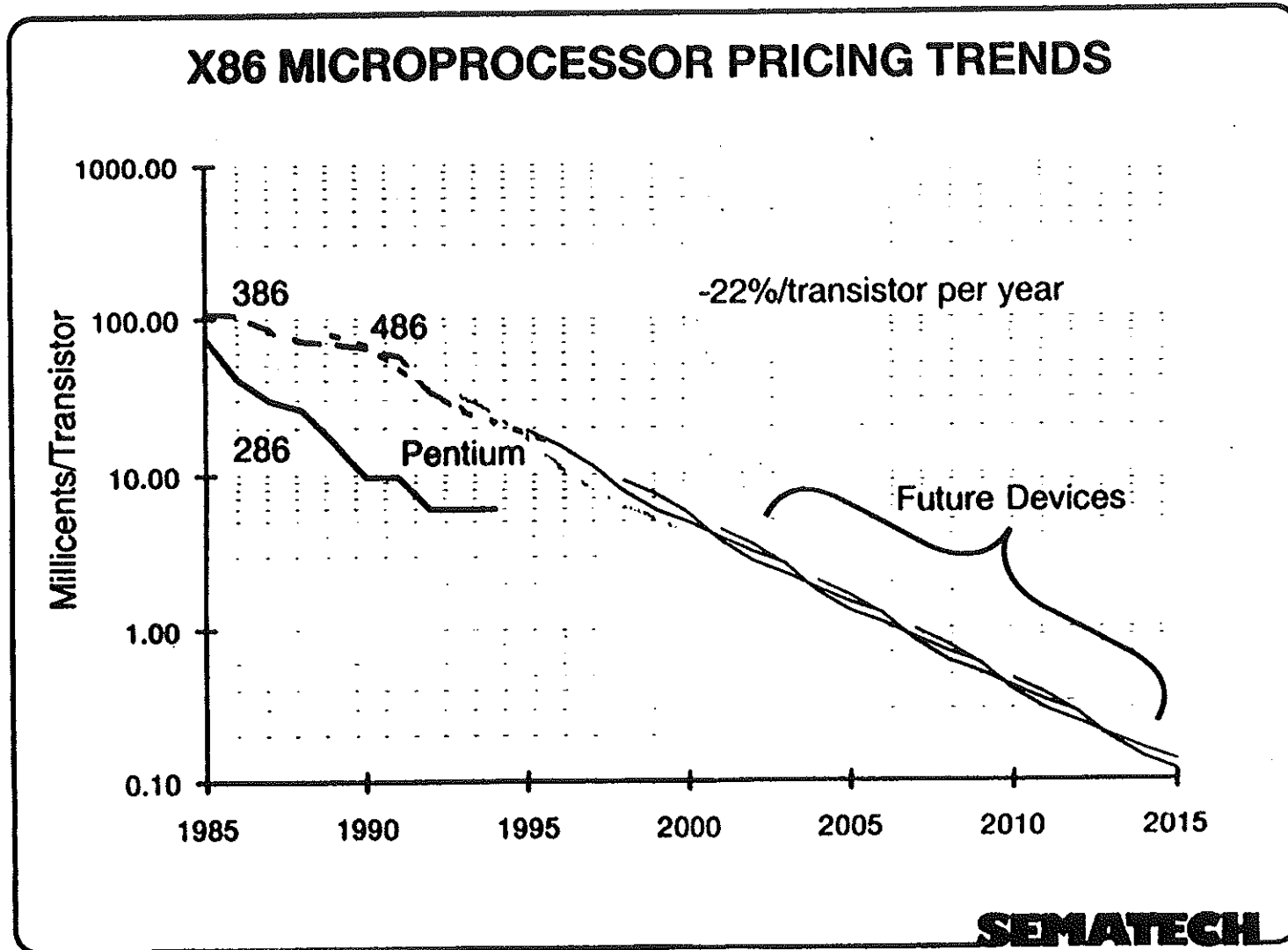
Source: Integrated Circuit Engineering Corp.

SEMI/SEMATECH
PARTNERED FOR SUCCESS

Wafer Fab Capitalization.

Building and Land	13%	\$195M
Improvements	17%	\$255M
Equipment	56%	\$840M
Installation	14%	\$210M
Total	100%	\$1,500M

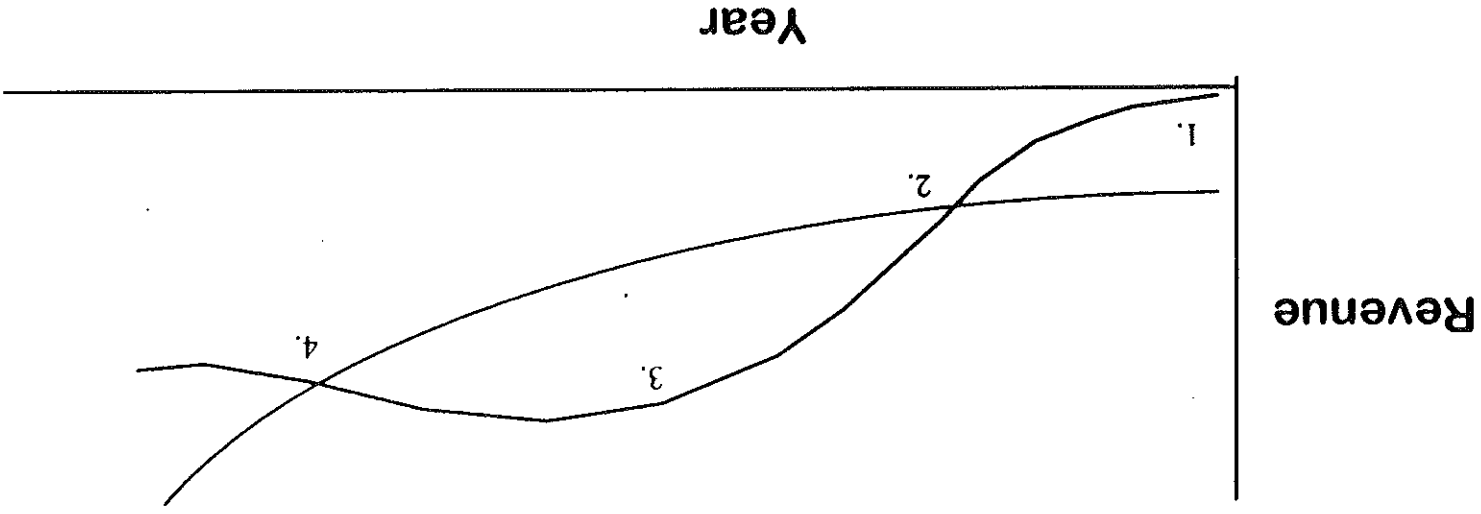
Average Selling Price (ASP).



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Semiconductor Business Cycles.

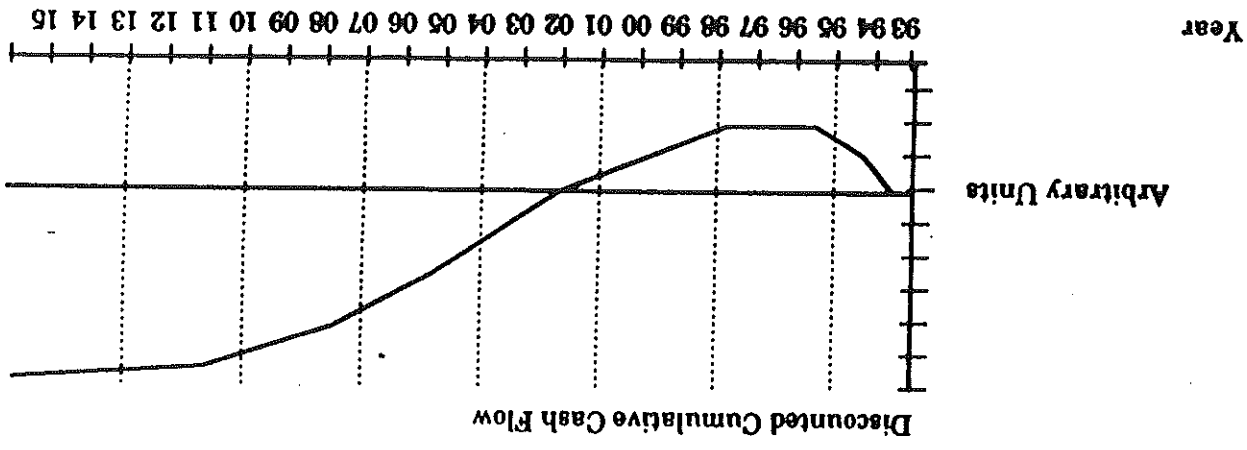
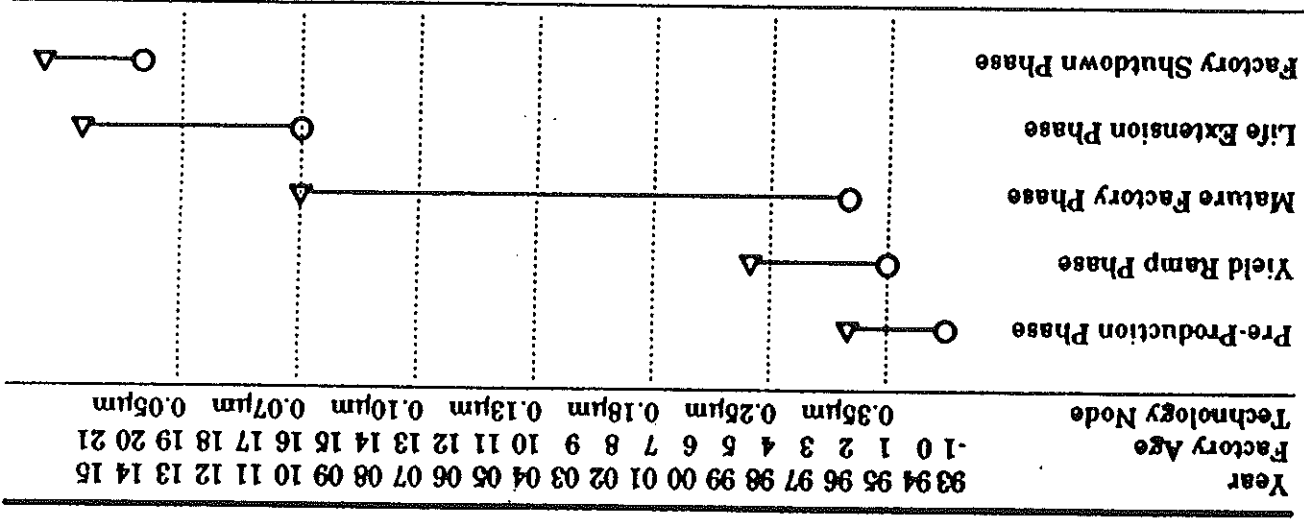


1. Process development/factory capability improvement.
2. Manufacturing ramp.
3. Sustained peak manufacturing capability.
4. Re-deployment of resources.

Semiconductor Wafer Fab Phases.

- **Pre-production.**
- **Yield ramp.**
- **Mature factory.**
- **Life extension.**
- **Shutdown.**

Semiconductor Wafer Fab Phases.



Process Life Cycles.

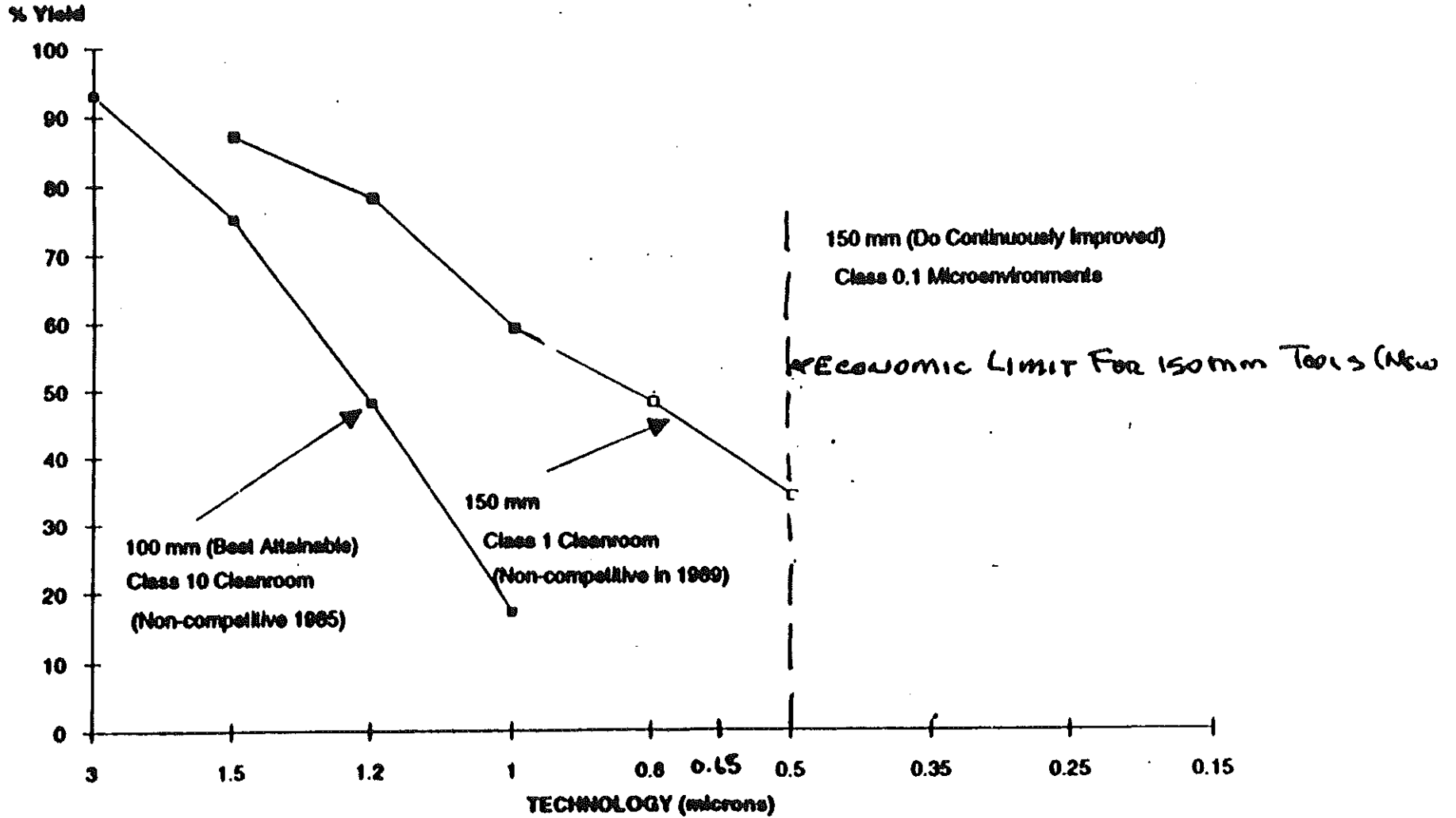
- **Specification.**
- **Design.**
- **New recipe development.**
- **Short loop processing.**
- **Full flow processing.**
- **Create recipes.**
- **Qualify.**
- **Yield ramp.**

Manufacturing Technology Changes.

PARAMETER	1995	1998	2001	2005
FEATURE SIZE	0.5	0.35	0.25	0.18 MICRONS
CHIP SIZE	400	500	600	700 MILS / SIDE
PROCESS COMPLEXITY (OF 1 MEG DRAM)	X 5	X 7	X 10	X 13
WAFER SIZE	8"	8"	8"	8" DIAMETER
STRUCTURE	THREE DIMENSIONAL CMOS AND BICMOS			
DRAM EQUIVALENCE	16 MB	64 MB	256 MB	1000 MB
TOOL SET CHANGES	INITIAL	#1	#2	#3
				NOT IN
				UPGRADE UPGRADE THIS FAB
				0.12
				0.18
				4000 MB

Factors Driving Change.

POTENTIAL YIELD VERSUS TOOL SET GENERATIONS



Technology Impact on Facility Design.

- FACILITY SHOULD HAVE A 12-YEAR LIFETIME, WITHOUT MAJOR UPGRADES.
- TOOLS WILL BE REPLACED SEVERAL TIMES, DURING THAT LIFETIME.
- MEANS THAT A FACILITY IN DESIGN TODAY SHOULD BE ABLE TO SUPPORT MICROELECTRONIC MANUFACTURING TO THE YEAR 2007.
- THIS SECTION LOOKS AT THE PROGRESSION IN MANUFACTURING EXPECTED BETWEEN 1990 AND 2000.
- THE MANUFACTURING FACILITY PERFORMANCE REQUIREMENTS ARE SET BY THE MANUFACTURING TECHNOLOGY EXPECTED IN THE YEAR 2000. THIS IS THE LIMIT OF TODAY'S KNOWLEDGE ON SPECIFICATIONS.

Wafer Processing Requirements (150 mm).

Energy Usage.....	285 kWh
Material Usage	89 lbs
Liquid Chemicals	63 lbs
Sodium Hydroxide (wastewater neutralization)	25 lbs
Hazardous Waste	7 lbs
Non-hazardous waste	82 lbs
Atmospheric Gases (3200 ft ³)	250 lbs
Water Usage	2,800 gallons
DI Water Usage.....	2,272 gallons

ESH Impact on the Cost of Ownership for a Tool.

- **Permitting by regulatory agencies.**
- **Electric power consumption.**
- **Storing, handling, and dispensing hazardous process materials.**
- **Selection of process materials.**
- **Efficiency of use of process materials.**
- **Exhaust air needed to carry away and dilute the gaseous wastes.**
- **Water and chemical treatment systems to neutralize liquid wastes.**
- **Abatement systems for gaseous wastes.**

Business Issues Having ESH Ramifications.

- **Semiconductor business cycles - effects timing and location.**
- **Semiconductor wafer fab phases - effects factory operation and ultimately restricts ability to change.**
- **Process life cycles - enables ability to change and drives much of the cost.**
- **Other issues - effect the sustainability of our industry growth.**

Semiconductor Business Cycles.

- **Time to market - includes start-up delay due to permits.**
- **Market access issues resulting from international directives and standards.**
- **Regional concerns.**

Semiconductor Wafer Fab Phases.

- **Size of factories imposing “new” high threshold requirements.**
- **Increased cost controls.**
- **Reduced risk factors.**

Process Life Cycles.

- **Characterization of process tool emissions.**
- **Chemical substitution opportunities.**
- **Waste minimization.**

Other Issues.

- **Changing regulatory environment.**
- **Improved knowledge of processes.**
- **International issues.**

Solutions.

- Design for Environment Safety and Health (DFESH).
 - DFESH is a systematic management approach for evaluating and mitigating ESH concerns at the earliest possible stages of process design or product life cycle. This includes:
 - Ongoing evaluation during the product life cycle
 - Optimizing balance between ESH priorities and competing factors:
 - √ Cost.
 - √ Convenience.
 - √ Schedule.
 - √ Product quality.
 - √ Performance.
 - Requires value judgment based on best information available.
- Industry coordination and cooperation.

Current Hot Issues.

- **Global warming.**
- **Water and waste minimization.**
- **Barriers to international competition.**
- **Worker safety.**

- Contacts for More Information.**
- Semiconductor Industry Association.
 - Semiconductor Safety Association.
 - SEMATECH.

Acknowledgments.

- **Jenni Carter and Glenn Fishler with E.O.R.M.**
- **Jerry Schoening with Applied Materials.**
- **Lee Neal with the Semiconductor Industry Association.**
- **Ray Kerby with SEMATECH.**
- **Joseph Fiskel with Decision Focus.**
- **Dona McCord with Radian D-Tech.**

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