Semiconductor International

Coping with the High Cost of Wafer Fabs

Flexibility is the byword for new fabs as the semiconductor industry heads toward the next century.

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Senior Editor

Key Technologies:

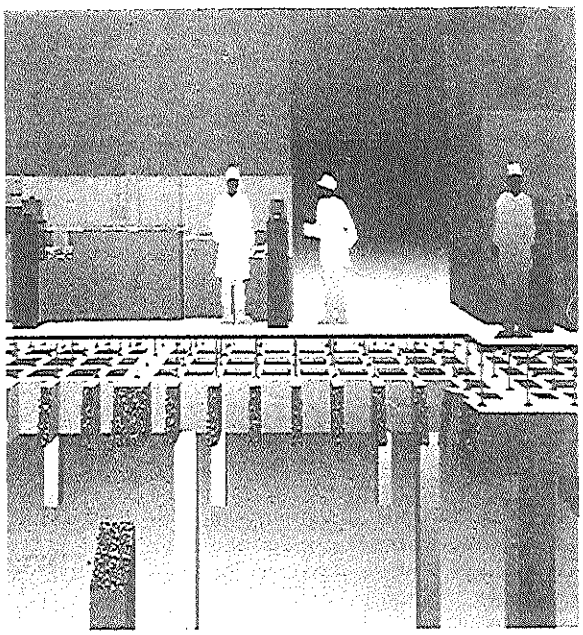
- Wafer Fab Designs
- Equipment Trends
- Automation Trends

At A Glance:

Manufacturing issues — all the subtle complexities that tie a company's investment in bricks and mortar to revenue — will play a key role in tomorrow's successful semiconductor fab. Equipment, process, and especially facilities strategies, must anticipate and address market and financial pressures for the year 2000. Short product life cycles will be demanded, requiring fast time to market, just-in-time manufacturing and on-time delivery, with parallel ramp-up of companion products. Flexibility to modernize a fab while sustaining high yields will also be necessary, along with an ability to economically change process flows and wafer sizes with virtually no disruption. Companies will be required to manufacture many designs, perhaps in multiple technologies, and in varying volume from a few thousand chips to many millions over the circuit design's life cycle.

Without a paradigm shift, issues surrounding capital investment and operating costs may cripple the semiconductor industry by the turn of the century. The common claim is that IC factories already cost more than $1 billion, accelerating toward $2 billion by 2000. At the 1994 Advanced Semiconductor Manufacturing Conference, one expert reported that by 2000 the required investment for new facilities could rise to an unacceptable 50% of revenues.

Professor Krishnar Saraswat at Stanford University (Stanford, Calif.) reported, "This trend has the potential to squeeze all but the largest, most vertically integrated firms out of the industry and to slow down technology innovation."



A "one story with basement" prototype in the Strategic Future Fab Study proved to be the most cost-effective of the four alternative designs proposed. (Source: Fluor Daniel)

The counterpoint is: Entering 1995, many IC manufacturers are still showing good, even a growing, return on investment. Perhaps the squeeze is on some smaller manufacturers, who are switching to silicon foundries.

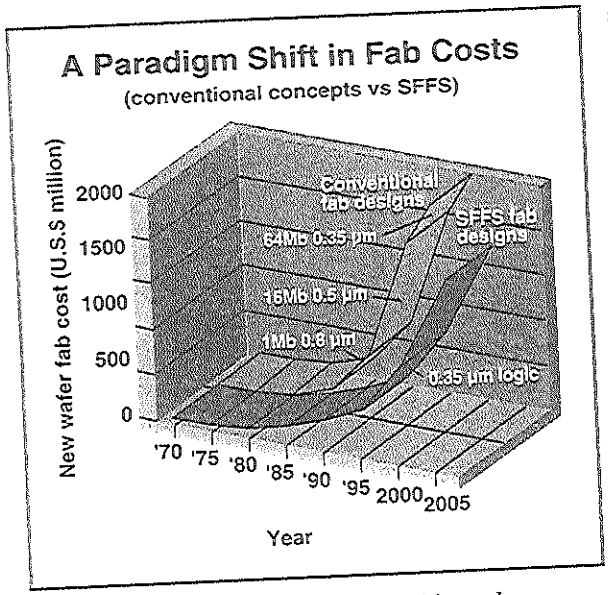
Beyond 2000, some experts believe the road may change dramatically, even before semiconductor manufacturing has to confront the fundamental limitations of silicon technology.

Is the expensive facility an isolated need? A rough poll taken by *Semiconductor International* shows that between 80 and 140 new wafer fabrication facilities will be needed by 2000.

Where does the money go?

On the bricks-and-mortar-side, the expense comes from building a manufacturing space inside a conventional ballroom cleanroom design. Most new fabs are drawn up with at least 65,000 ft² of Class 1 or better cleanroom space. Some of these expensive fabs, particularly for DRAM manufacturing, have a useful life of only about three years.

A typical new fab may call for hundreds of large, different pieces of equipment costing up to $4 million a copy. Integrated Circuit Engineering (ICE) reports that in the mid-1990s



1. The Strategic Future Fab Study (SFFS) focused on designing and equipping semiconductor manufacturing facilities that provide a paradigm shift from the soaring costs of conventional fab designs. (Source: Fluor Daniel)

65% of new wafer fab facility costs will be equipment costs (Fig. 1). Experts interviewed by *Semiconductor International* say we are quickly approaching 75%.

Not completely separate from the overall problem, wafer processing equipment has its own subset of complex challenges. Automation standards are not where they need to be and many process equipment solutions are relatively fixed manufacturing configurations. Malcolm Williams at Fluor Daniel says, "We believe that intrabay automation is too inflexible; it's difficult to change through software redesign."

Semiconductor manufacturing is also being driven by community issues such as environmental and safety responsibilities, and even employment opportunities.

The best wisdom in the industry says that continued use of conventional standalone equipment in a ballroom-type fab design means that costs will accelerate at an unhealthy pace. Paul Castrucci of Castrucci & Associates is an industry ombudsman for a paradigm shift. "We need fab designs that give better flexibility and extendability; the industry needs to get on a new curve," he says.

Continuing work...

Current thinking about manufacturing design can draw on a significant amount of recent research. One of the most visible efforts was done in Texas Instruments' MMST (Microelectronics Manufacturing Science and Technology) program, which was supported by government funding and done in contract with Stanford University, Applied Materials, IPEC and Gasonics. This program looked at the technical feasibility of the following:

- 100% single wafer processing, including total rapid thermal processing;
- 95% dry processing;
- real-time model-based process control;
- in-situ sensors; dynamic, distributed, seamless, object-oriented CIM, based on a real-time factory model;
- integrated minienvironments; and
- truly modular systems.

The MMST program came up with a flexible semiconductor manufacturing fab design that enabled the running of different process flows on successive wafers. Its crowning achievement was a three-day cycle time using a double metal 0.35 µm CMOS process.

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Portions of this work continue at Stanford University in its Programmable Factory project. This is an interdisciplinary program aimed at building a highly flexible computer-controlled manufacturing facility and a suite of virtual factory simulation tools that emulate all functions of a real factory.

Stanford researchers are developing a new class of multifunctional equipment. Classified as rapid thermal processing, this equipment can quickly process one wafer at a time, performing several process steps in-situ. Single wafer processing enables the use of in-situ monitoring and real-time control. The process equipment is also modular, with common mechanical and electronic interfaces. Modularization and standardization are expected to decrease the amount and expense of equipment that must be purchased for existing fabs to upgrade to new generations of technology.

SEMATECH's future factory

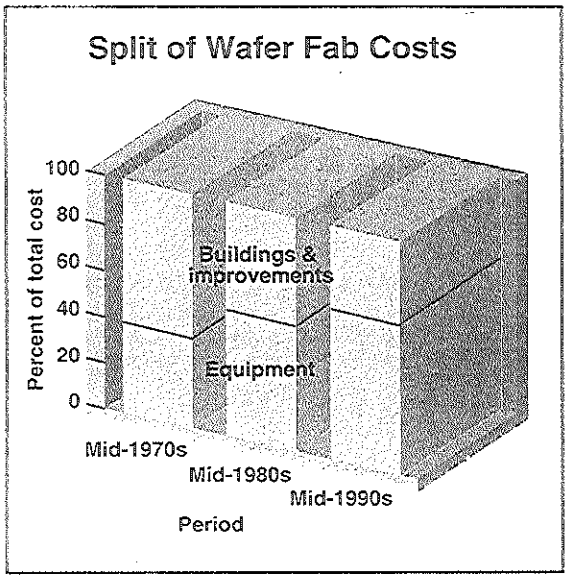
Engineers at SEMATECH have also looked at other aspects of future fab needs. Some of its most significant efforts include fab layout software, cost-of-ownership modeling software, and standards for equipment installation and subsystems. Much of the work at SEMATECH involves fab design modeling that explores process flows, wafers per lot, wafer diameters and minienvironments. SEMATECH now has a complete facilities cost model that allows estimation of costs by type of fab and even by geographic region.

SEMATECH engineers, working in conjunction with Industrial Design Corp. (Portland, Ore.), identified ways to reduce construction costs associated with fabs. A summary of this work reports that fab facility costs are determined to a large extent early on in a project by decisions concerning the amount of space required for manufacturing operations, support utility requirements, site locations and lease strategies. Various ways to reduce facility costs from 5-15%, with minimal or no impact on a manufacturing operation, were identified.

Strategic Future Fab Study

One *complete* look at the semiconductor factory of the future has come from the Strategic Future Fab Study (SFFS). Fluor Daniel, an engineering and construction company, sponsored and led the SFFS, retaining Paul Castrucci & Associates to provide direction. SFFS tapped the knowledge of various consultants, as well as semiconductor equipment, materials and software suppliers (Table 1). NCR (Ft. Collins, Colo.) served as the client IC manufacturer in this study.

The participants in SFFS set off to develop a new standard in fab design for submicron wafer processing, challenging the conventional Class 1 ballroom design. They studied four alternative wafer fabrication facility concepts:



2. For a new semiconductor facility, the split between building and equipment costs is steadily shifting. (Source: ICE)

- a "new fab standard" using Class 1 minienvironments;
- a conventional, but smaller, Class 1 "ballroom";
- a "one story with basement" small footprint facility using Class 1 minienvironments; and
- a two story "slab-on-grade" using Class 1 minienvironments.

The metrics to evaluate these designs were reductions in capital investment, time to market, wafer processing costs, wafer cycle time, and yield learning time, along with environmental responsibility and manufacturing facility lifetime flexibility. The target process was 0.35 μm CMOS with 19 masks and four levels of metal for 500, 200 mm wafer starts per day, and a facility set to manufacture a minimum of 25 IC types in seven days or less.

What SFFS revealed

The reality of SFFS is that it uses today's technology with some twists that may counter conventional wisdom. Its "technology enablers" include integration of minienvironments with maximum use of cluster tools. This provides the most cost-efficient and profitable wafer fab design. The study's most cost-efficient and profitable fab uses integrated cluster tools in Class 1 minienvironments inside Class 10,000 work spaces. The minienvironment-cluster tool combination, they found, is the best solution for providing less than 0.05 defects per square centimeter.

SFFS shows that enablement benefits come with maximum use of CIM, advanced yield management, "smart tag" logistics control, and computer-based manufacturing simulation technology and advanced production control, capable of presenting a 3-D simulation of a virtual factory. Simulation and scheduling software provide the 'knowledge' to drive cycle time to under two times the raw process time.

This simulation revealed that aggressive cycle time has to be maintained for both engineering and production to achieve time-to-market goals. Simulation showed that favorable cycle time comes with

- a dedication of tool sets to single process steps where practical, and
- redundancy in each equipment type whose failure could shut down the line.

In all four SFFS designs, costs fall below $4 per square centimeter of silicon within a year.

The manufacturing simulation used in SFFS showed that optimum cycle time requires the use of backup equipment at each operation, using either a minimum tool set of two or more systems, or an individual system where a simple setting change provides nearly identical process results.

Other conclusions from SFFS that help reduce equipment and processing costs include:

- using test wafers and monitoring root causes of in-line parametric data variation,
- installing systems capable of multiple processes,
- integrating steppers to their coat-and-develop systems,
- mixing i-line and deep-UV lithography and dedicating groups of lithography tools to several mask operations,
- using cluster tools for multilayer deposition and etch in a single machine, and
- using SMIF enclosures on all equipment, including reticle storage facilities.

SFFS showed that significant improvements in manufacturing and production facility design, construction and operation are possible using key technologies and concepts. For example, minienvironments provide minimum disruption and built-in flexibility to allow modernization through several generations of product while maintaining wafer throughput and product yield during equipment installation and retooling.

Ongoing cost savings from minienvironment-based fab designs were found to be a result of several factors: Lower air flow requirements allow reduced electrical power consumption. Less stringent cleanliness conditions reduce garmenting costs and dressing time. Cycle times of six days, rather than 60-90 days, minimize work in progress inventory. Yield learning time is found to be one year compared to the conventional two years, driving earlier revenue growth.

All four designs analyzed by SFFS also have acceptable manufacturing costs. Within a year of the start of production, costs fall below $4/cm^2 of silicon. All four designs show lower than conventional construction costs and have acceptable (greater than 9%) return on investment — that pay for themselves in 24 months or less.

In terms of time to market, all four designs are considerably faster than traditional methods. The best scenario provides a production facility in 18 months from the start of engineering design — four months sooner than the traditional Class 1 ballroom cleanroom.

Castrucci says, "SFFS has shown that it is possible to meet or exceed the SIA 1993 Roadmap Study benchmark targets for cost and scheduling." Such a fab, he notes, can generate nearly $12,000 of revenue per wafer in the second year of production startup. And the designs lend themselves to upgrade through multiple product generations without significant interruptions in product yield. This represents a paradigm shift in wafer processing.

While some of the concepts out of SFFS are being used at NCR, the

Table 1. Members of the Partnering Team Participating in the Fluor Daniel Strategic Future Fab Study

Company	Products and expertise	Circle No.
Air Products and Chemicals	High purity bulk and specialty gases, equipment, materials and services	328
Amray	Electron microscope systems for wafer inspection and metrology	329
Applied Materials	Ion implantation, deposition and etching systems	330
Applied Chemical Solutions*	Chemical generation and distribution systems	331
Asyst Technologies	Integrated minienvironment systems for wafer and reticle protection	332
AutoSimulations	Factory simulation and scheduling software	333
Wm. Blackwell A.I.A.	Architectural consulting	334
Paul Castrucci & Associates	Consultants to the semiconductor industry	335
FASTech Integration	Factory automation software solutions	336
Fluor Daniel	Factory engineering and construction	337
Integrated Circuit Engineering	Business and market consulting, laboratory analysis, and training	338
International Business Consulting	Business and financial consulting	339
IPEC Westech	Chemical-mechanical polishing	340
KLA Instruments	Yield management and process control systems	341
LPA Software	Equipment and factory automation solutions	342
Nicoson Consulting	Industrial engineering and technology	343
Penfield Liquid Treatment Systems	Ultrapure water generation systems	344
Premiere Hi-Tech	Semiconductor industry consulting and training	345
Proconics International**	Automated wafer lot, reticle and materials control systems and software	346
Silicon Valley Group	Lithography, resist processing, oxidation, diffusion and LPCVD	347
Submicron Systems	Wet chemistry processing systems	348
Ultratech Stepper	Lithography exposure systems	349

*acquisition by FSI International pending final approval
**now Asyst Automation

SFFS results are new, and all concepts have not yet been tested in an actual facility.

Bill Barnett, Fluor Daniel business development director, says, "Clearly, our study has identified some promising strategies for future fabs. However, we believe that additional capital and operational cost benefits exist that have not yet been quantified and communicated. We are in the process of analyzing these."

The future...

Clearly, the rising cost of continually building new semiconductor manufacturing facilities is dictating a new direction for the immediate future — a paradigm shift. But the options, at least many of them, seem to be in place. By 2000, a wafer fab facility will be highly automated. Software simulation and scheduling will set the direction. Software control will evaluate and decide. And minienvironments and the equipment itself will be the cleanroom. □

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